



# Lattice Timing Training

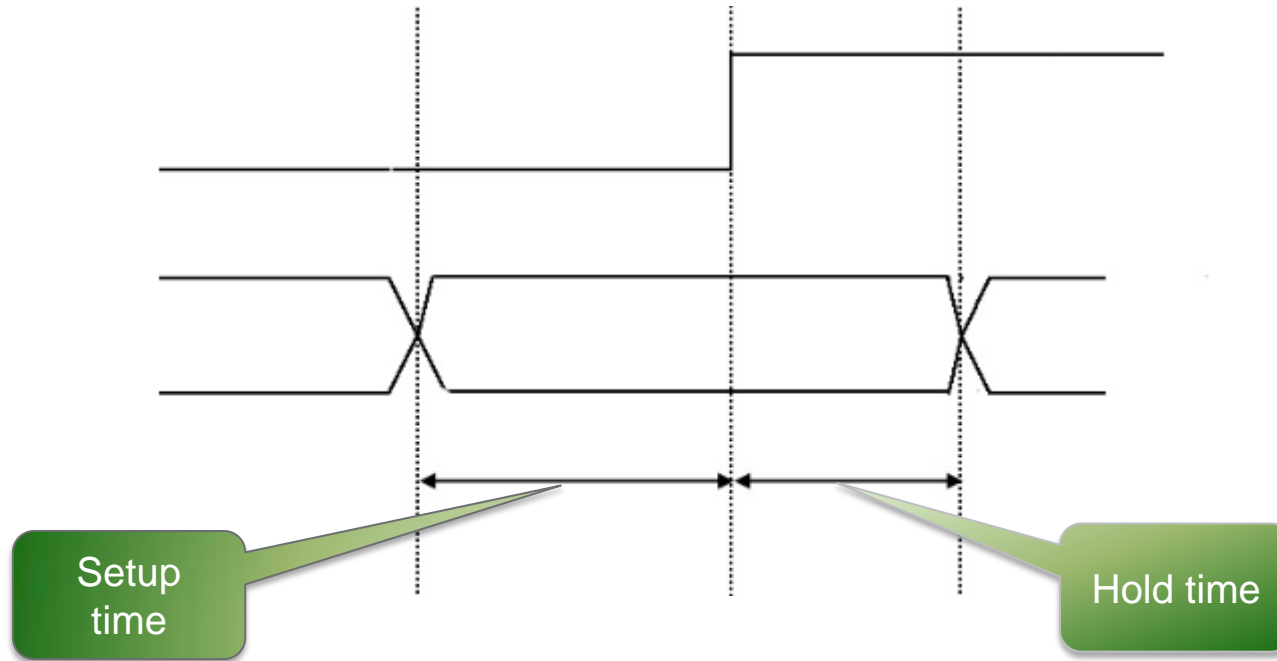
LATTICE

**DIAMOND**

DESIGN SOFTWARE

- **Constraints**
  - Setup and hold time concept.
  - Frequency constraint.
  - Input setup constraint.
  - Clock to out constraint.
  - Max delay constraint.
  - Multi cycle constraint.
  - Block constraint.
- **Coding style**
- **Methods of timing closure.**

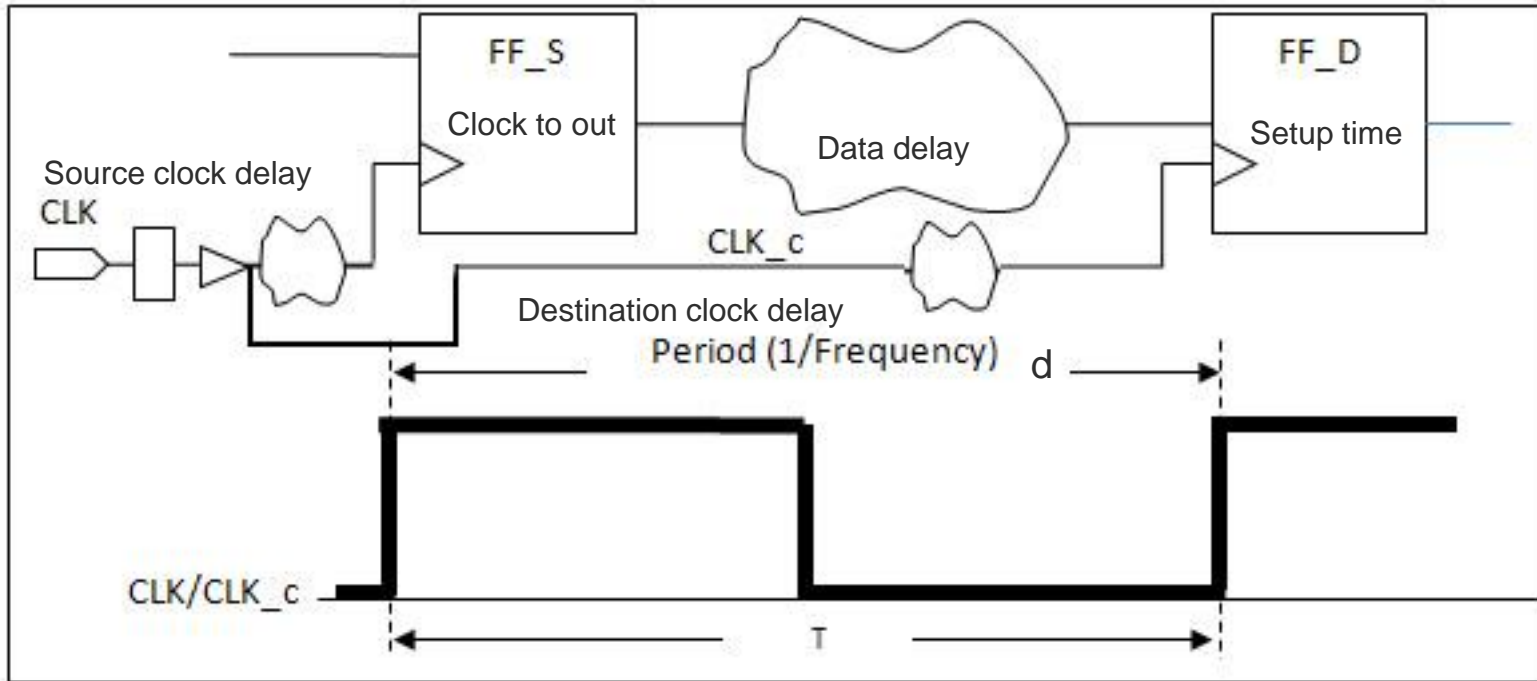
# SETUP AND HOLD TIME CONCEPT



Note: Two description:

1. Register need mini setup time and mini hold time.
2. Provide how many setup time and hold time for register.

# FREQUENCY CONSTRAINT



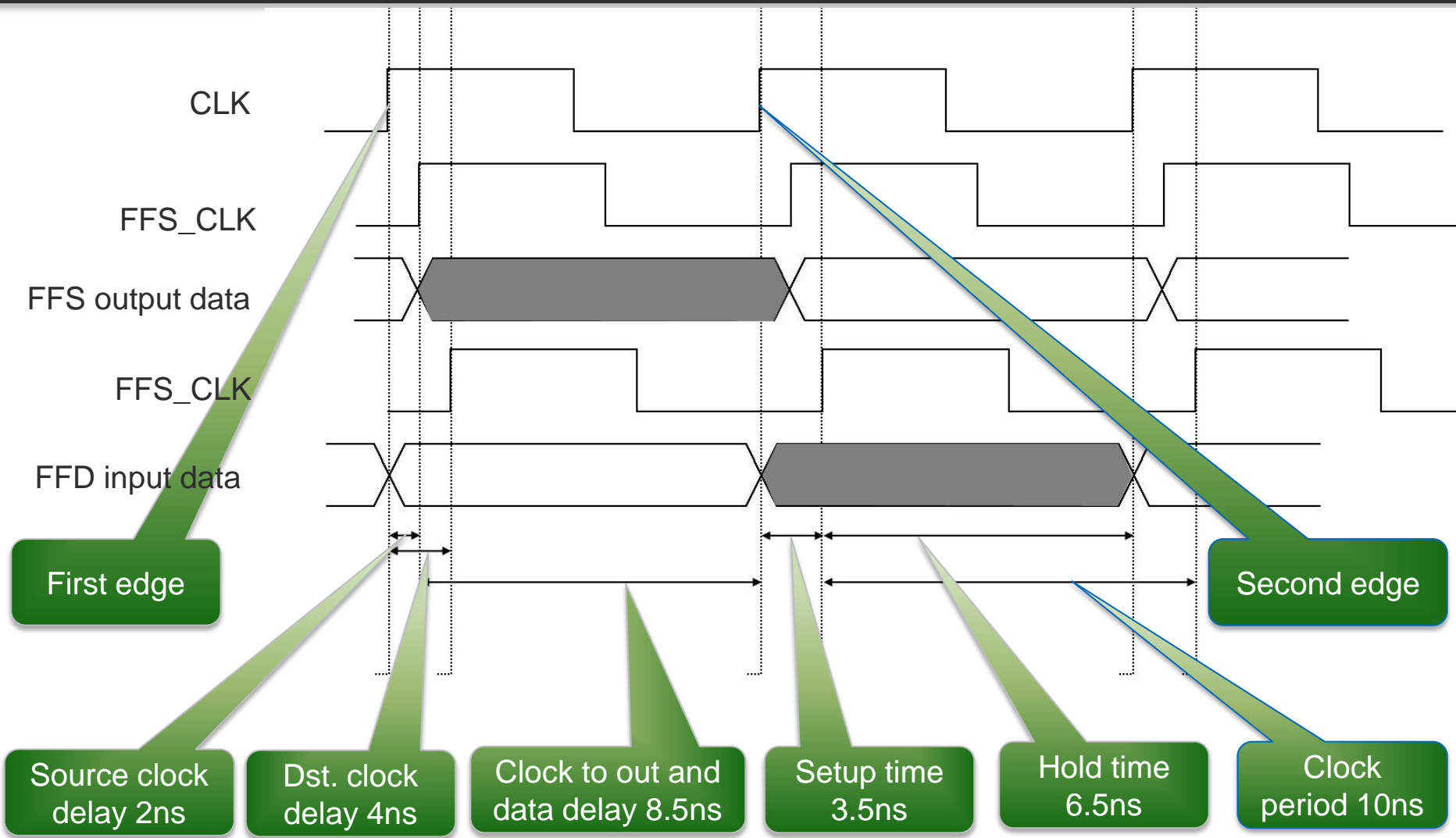
- Source clock delay(SCLKT) = 2ns.
- Clock to out(CTO) = 0.5 ns.
- Data delay(DT) = 8 ns.
- Destination clock delay(DCLKT) = 4 ns
- Mini setup time(ST)(FF require) = 0.2 ns.
- Clock period(T) = 10 ns.
- Mini hold time(HT) = 0 ns.
- Clock skew = SCLKT – DCLKT = -2ns.

Calculate: Setup time and Hold time of FF\_D.

$$\begin{aligned} \text{Setup time} &= T - \text{Skew} - (\text{CTO} + \text{DT}) \\ &= 10 - (-2) - (0.5 + 8) = 3.5 \text{ ns.} \end{aligned}$$

$$\begin{aligned} \text{Hold time} &= T - \text{Setup time} \\ &= T - (T - \text{Skew} - (\text{CTO} + \text{DT})) \\ &= \text{Skew} + (\text{CTO} + \text{DT}) \\ &= -2 + (0.5 + 8) = 6.5 \text{ ns.} \end{aligned}$$

# TIMING WAVE



# CALCULATE FMAX

- Source clock delay(SCLKT) = 2ns.
- Clock to out(CTO) = 0.5 ns.
- Data delay(DT) = 8 ns.
- Destination clock delay(DCLKT) = 4 ns
- Mini setup time(ST) = 0.2 ns.
- Clock period(T) = 10 ns.
- Mini hold time(HT) = 0 ns.
- Clock skew = SCLKT – DCLKT = -2ns.

Calculate: Setup time and Hold time of FF\_D.

$$\begin{aligned}\text{Setup time} &= T - \text{Skew} - (\text{CTO} + \text{DT}) \\ &= 10 - (-2) - (0.5 + 8) = 3.5 \text{ ns.}\end{aligned}$$

$$\begin{aligned}\text{Hold time} &= T - \text{Setup time} \\ &= T - (T - \text{Skew} - (\text{CTO} + \text{DT})) \\ &= \text{Skew} + (\text{CTO} + \text{DT}) \\ &= -2 + (0.5 + 8) = 6.5 \text{ ns.}\end{aligned}$$

$$\text{ST} = T - \text{Skew} - (\text{CTO} + \text{DT})$$



$$\begin{aligned}T &= \text{ST} + \text{Skew} + (\text{CTO} + \text{DT}) \\ &= \text{Mini setup time} + \text{Skew} + \text{Clock to out} + \text{Data delay.}\end{aligned}$$



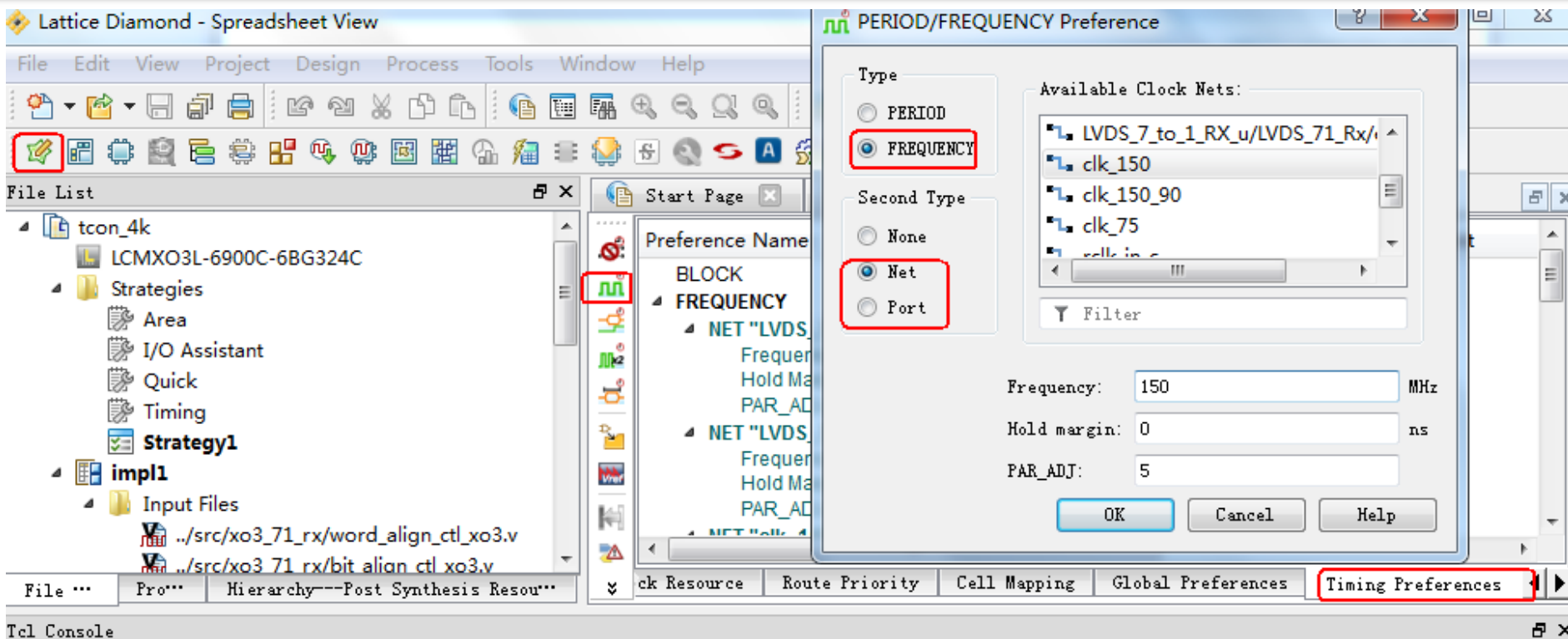
$$\text{FMAX} = 1/T.$$

Example:

$$\begin{aligned}0.2 &= T - 2 - (0.5 + 8) \\ T &= 0.2 + (-2) + (0.5 + 8) = 6.7 \text{ ns}\end{aligned}$$

$$\text{FMAX} = 1/T = 1/6.7 = 149 \text{ MHz.}$$

# ADD FREQUENCY CONSTRAINT



The screenshot shows the Lattice Diamond Spreadsheet View interface. The 'PERIOD/FREQUENCY Preference' dialog box is open, with the following settings:

- Type:  FREQUENCY
- Second Type:  Net
- Available Clock Nets: LVDS\_7\_to\_1\_RX\_u/LVDS\_71\_Rx/, clk\_150, clk\_150\_90, clk\_75, clk\_in
- Frequency: 150 MHz
- Hold margin: 0 ns
- PAR\_ADJ: 5

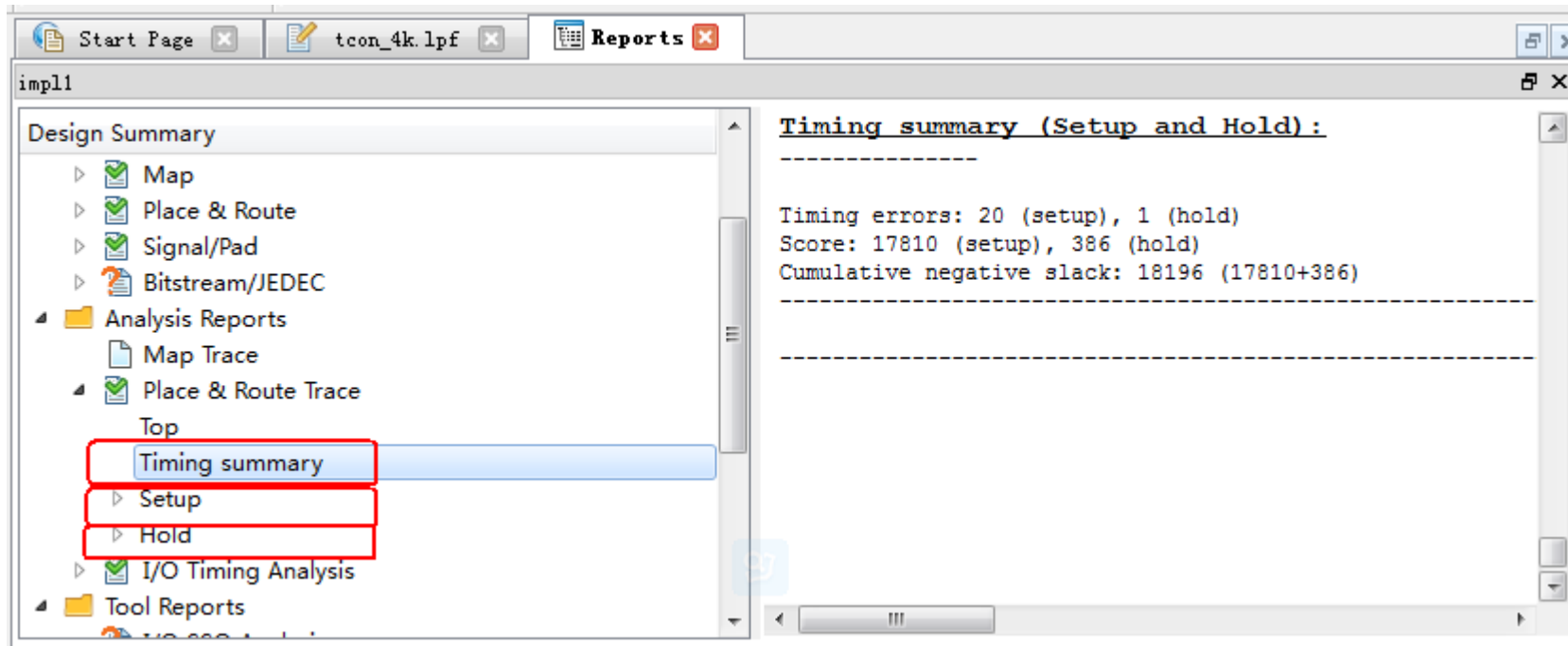
The 'Timing Preferences' tab is selected in the bottom right corner of the dialog box. The 'Tcl Console' at the bottom shows the command: `> prj_project open "D:/diamond_training/Demo/tcon_4k_v28/par/tcon_4k.1df"`

Click Spreadsheet > Click Timing preferences > Period/frequency >

After click OK button, the preference will be added in LPF file. Such as:

```
FREQUENCY NET "clk_150" 150.000000 MHz PAR_ADJ 5.000000 ;
```

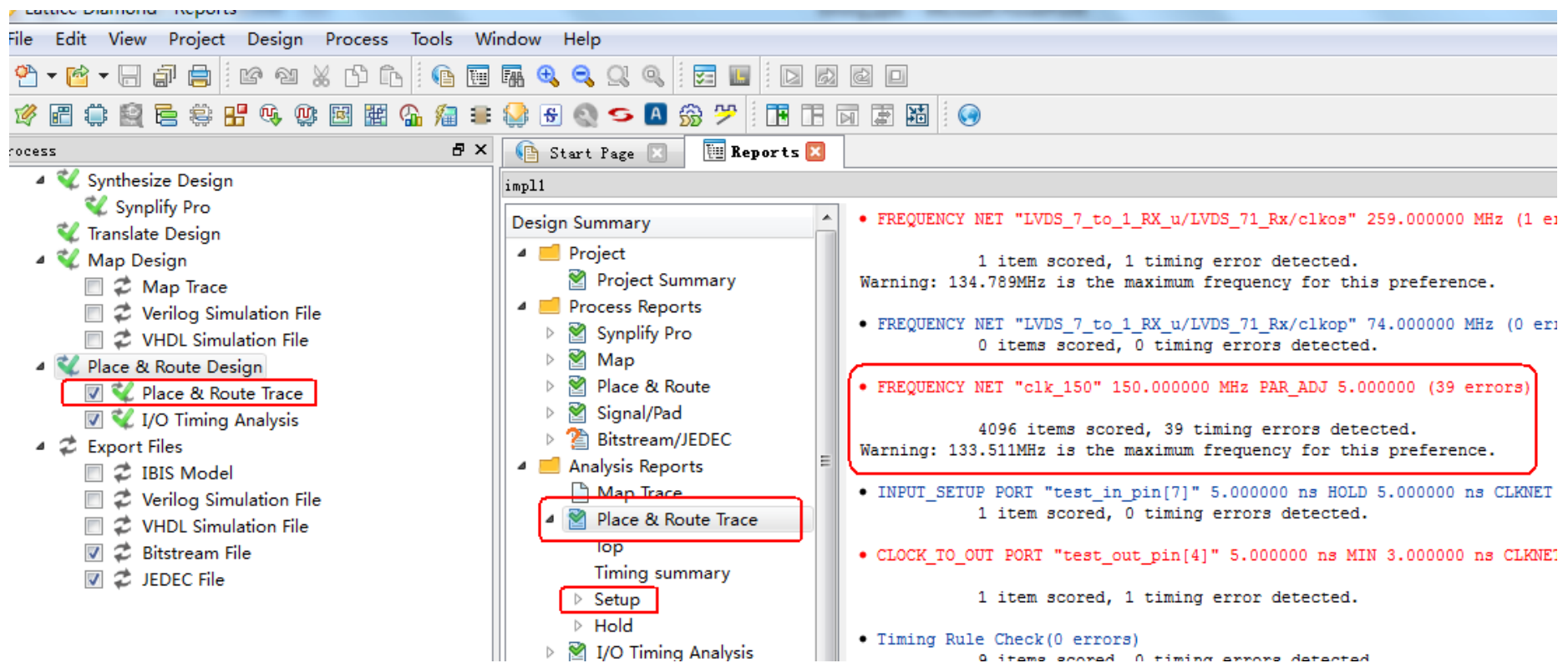
# CHECK TRACE REPORT



- Timing errors report how many paths can't meet timing constraint.
- Score is smaller, timing is better, if all timing meet, the score is zero.



# SETUP TIME REPORT



The screenshot shows the Lattice Diamond Reports window. The left pane displays the project tree with the following items:

- Synthesize Design
  - Synplify Pro
- Translate Design
- Map Design
  - Map Trace
  - Verilog Simulation File
  - VHDL Simulation File
- Place & Route Design
  - Place & Route Trace (highlighted with a red box)
  - I/O Timing Analysis
- Export Files
  - IBIS Model
  - Verilog Simulation File
  - VHDL Simulation File
  - Bitstream File
  - JEDEC File

The right pane shows the Design Summary for 'impl1'. The 'Place & Route Trace' item is highlighted with a red box. The report content includes the following items:

- FREQUENCY NET "LVDS\_7\_to\_1\_RX\_u/LVDS\_71\_Rx/clkos" 259.000000 MHz (1 error)  
1 item scored, 1 timing error detected.  
Warning: 134.789MHz is the maximum frequency for this preference.
- FREQUENCY NET "LVDS\_7\_to\_1\_RX\_u/LVDS\_71\_Rx/clkop" 74.000000 MHz (0 errors)  
0 items scored, 0 timing errors detected.
- FREQUENCY NET "clk\_150" 150.000000 MHz PAR\_ADJ 5.000000 (39 errors)  
4096 items scored, 39 timing errors detected.  
Warning: 133.511MHz is the maximum frequency for this preference.
- INPUT\_SETUP PORT "test\_in\_pin[7]" 5.000000 ns HOLD 5.000000 ns CLKNET  
1 item scored, 0 timing errors detected.
- CLOCK\_TO\_OUT PORT "test\_out\_pin[4]" 5.000000 ns MIN 3.000000 ns CLKNET  
1 item scored, 1 timing error detected.
- Timing Rule Check(0 errors)  
0 items scored, 0 timing errors detected.

- Trace report is txt file, expanded-name is twr.
- Red line mean timing can't be meet.

# SETUP TIME REPORT

Preference: FREQUENCY NET "clk\_150" 150.000000 MHz PAR\_ADJ 5.000000 ;  
 4096 items scored, 39 timing errors detected.

---

Error: The following path exceeds requirements by 0.823ns

Logical Details:	Cell type	Pin type	Cell/ASIC name	(clock net +/-)
Source:	FF	Q	tcon_sub_u/hs_cnt[6]	(from clk_150 +)
Destination:	FF	Data in	tcon_sub_u_gckio	(to clk_150 +)
Delay:	7.467ns (26.8% logic, 73.2% route), 5 logic levels.			

## Constraint Details:

7.467ns physical path delay tcon\_sub\_u/SLICE\_80 to gck\_MGIOL exceeds  
 6.667ns delay constraint less  
 -0.098ns skew and  
 0.121ns DO\_SET requirement (totaling 6.644ns) by 0.823ns

Skew = Source Clock Delay - Destination Clock Delay = 1.560 - 1.658 = -0.098ns.  
 6.667(T)-(-0.098)(skew)-0.121(Mini set time) = 6.644ns.(Be allowed max data delay)  
 7.467 - 6.664 = 0.823ns. (Exceed time)

# SETUP TIME REPORT

## Physical Path Details:

Data path tcon\_sub\_u/SLICE\_80 to gck\_MGIOL:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.367	R12C15D.CLK to	R12C15D.Q1 tcon_sub_u/SLICE_80 (from clk_150)
ROUTE	8	1.614	R12C15D.Q1 to	R12C8D.C1 tcon_sub_u/hs_cnt[6]
CTOF_DEL	---	0.408	R12C8D.C1 to	R12C8D.F1 SLICE_794
ROUTE	4	0.857	R12C8D.F1 to	R12C12D.D1 tcon_sub_u/N_24
CTOF_DEL	---	0.408	R12C12D.D1 to	R12C12D.F1 SLICE_797
ROUTE	1	0.351	R12C12D.F1 to	R12C12D.C0 tcon_sub_u/N_43
CTOF_DEL	---	0.408	R12C12D.C0 to	R12C12D.F0 SLICE_797
ROUTE	1	0.843	R12C12D.F0 to	R12C8D.D0 tcon_sub_u/gck5_i_3
CTOF_DEL	---	0.408	R12C8D.D0 to	R12C8D.F0 SLICE_794
ROUTE	1	1.803	R12C8D.F0 to	IOL_L24C.OPOS tcon_sub_u.N_433_i (to clk_150)

-----  
7.467 (26.8% logic, 73.2% route), 5 logic levels.

Data delay = Logic delay + Routing delay

# SETUP TIME REPORT

## Clock Skew Details:

Source Clock Path txpll\_u/PLLInst\_0 to tcon\_sub\_u/SLICE\_80:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	605	1.560	RPLL.CLKOP to	R12C15D.CLK clk_150
-----				
1.560 (0.0% logic, 100.0% route), 0 logic levels.				

Destination Clock Path txpll\_u/PLLInst\_0 to gck\_MGIOL:

Name	Fanout	Delay (ns)	Site	Resource
ROUTE	605	1.658	RPLL.CLKOP to	IOL_L24C.CLK clk_150
-----				
1.658 (0.0% logic, 100.0% route), 0 logic levels.				

Warning: 133.511MHz is the maximum frequency for this preference.

$$T = ST + Skew + (CTO+DT) = 0.121 + (-0.098) + 7.467 = 7.49ns.$$

$$FMAX = 1/T = 1/7.49 = 133.511MHz.$$

# HOLD TIME REPORT

```
Preference: FREQUENCY NET "clk_150" 150.000000 MHz PAR_ADJ 5.000000 ;  
4096 items scored, 0 timing errors detected.
```

---

Passed: The following path meets requirements by 0.296ns

```
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)  
  
Source: FF Q rd_addr[0] (from clk_150 +)  
Destination: PDPW8KC Port linebuf_u2/linebuf_0_0_2(ASIC) (to clk_150 +)  
  
Delay: 0.422ns (31.5% logic, 68.5% route), 1 logic levels.
```

## Constraint Details:

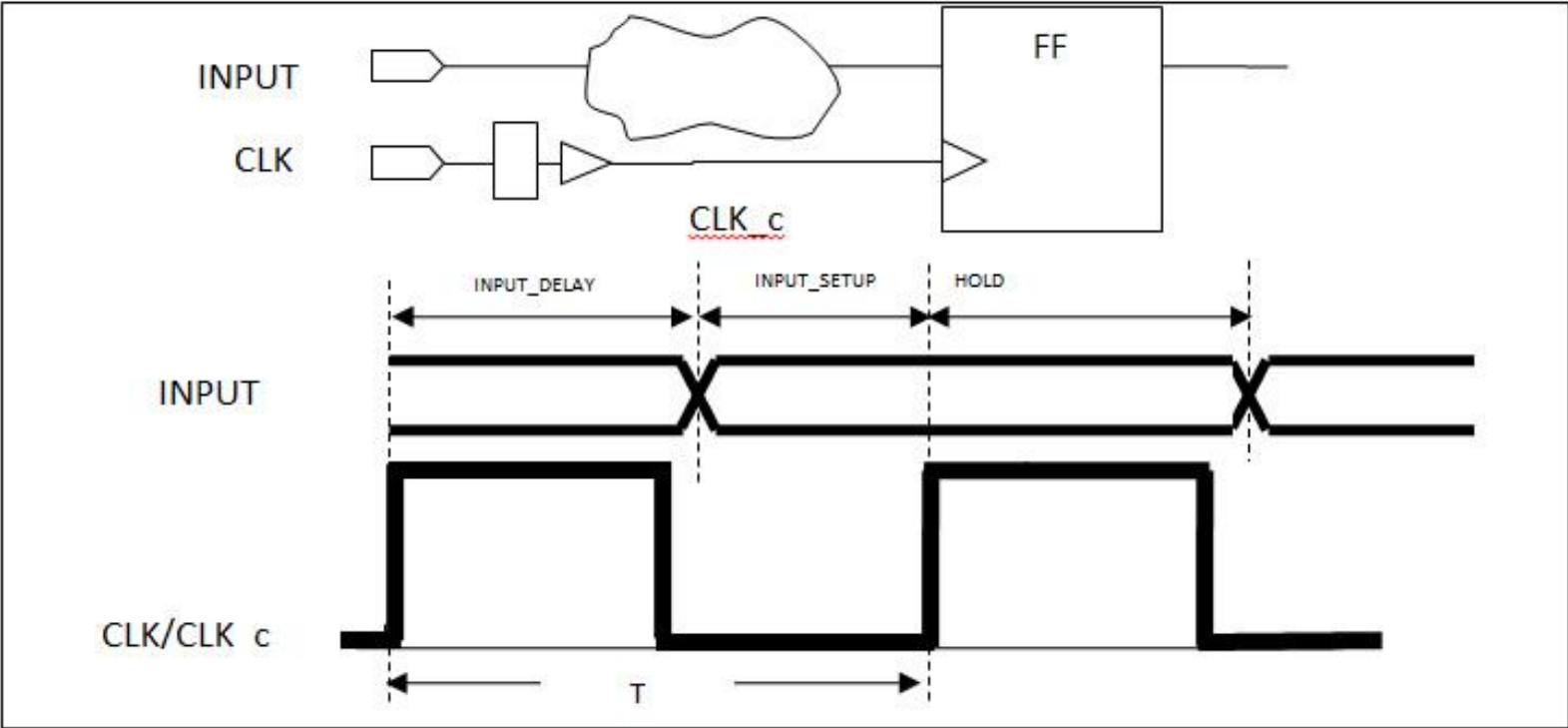
```
0.422ns physical path delay SLICE_0 to linebuf_u2/linebuf_0_0_2 meets  
0.072ns ADDR_HLD and  
0.000ns delay constraint less  
-0.054ns skew requirement (totaling 0.126ns) by 0.296ns
```

Hold time = Skew + (CTO+DT).

CTO+DT = Mini hold time - Skew = 0.072 - (-0.054) = 0.126ns.(Be allowed mini data delay).

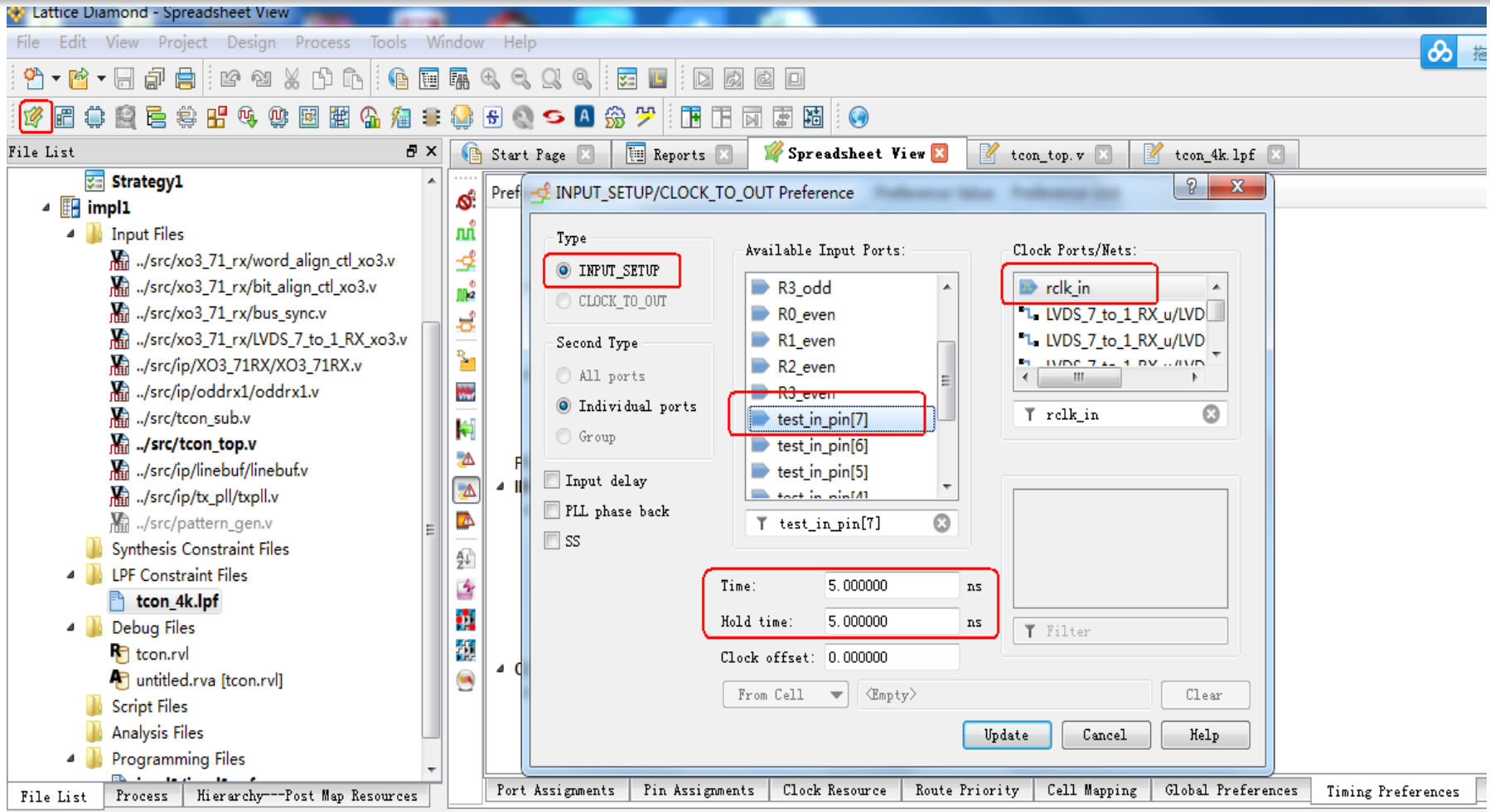
0.422 - 0.126 = 0.296ns.

# INPUT SETUP CONSTRAINT



$$\text{Input delay} + \text{input setup} = T$$

# ADD INPUT SETUP CONSTRAINT



The screenshot shows the Lattice Diamond Spreadsheet View interface. The 'INPUT\_SETUP/CLOCK\_TO\_OUT Preference' dialog box is open, showing the following settings:

- Type:  INPUT\_SETUP
- Second Type:  Individual ports
- Available Input Ports: test\_in\_pin[7] (highlighted)
- Clock Ports/Nets: rclk\_in (highlighted)
- Time: 5.000000 ns
- Hold time: 5.000000 ns
- Clock offset: 0.000000

The 'Update' button is highlighted in blue.

Click Spreadsheet > Click Timing preferences > input setup/clock to out >

```
INPUT_SETUP PORT "test_in_pin[7]" 5.000000 ns HOLD 5.000000 ns CLKPORT "rclk_in" ;
```

# SETUP TIME REPORT

Preference: INPUT\_SETUP PORT "test\_in\_pin[7]" 5.000000 ns HOLD 5.000000 ns CLKPORT "rclk\_in" ; Setup Analysis.  
1 item scored, 0 timing errors detected.

-----

Passed: The following path meets requirements by 5.373ns

Logical Details:	Cell type	Pin type	Cell/ASIC name	(clock net +/-)
Source:	Port	Pad	test_in_pin[7]	
Destination:	FF	Data in	test_in_reg_0io[7]	(to rclk_in_c +)
Max Data Path Delay:	2.327ns	(59.0% logic, 41.0% route),	1 logic levels.	
Min Clock Path Delay:	2.958ns	(36.7% logic, 63.3% route),	1 logic levels.	

#### Constraint Details:

2.327ns delay test\_in\_pin[7] to SLICE\_1097 less  
5.000ns offset test\_in\_pin[7] to rclk\_in (totaling -2.673ns) meets  
2.958ns delay rclk\_in to SLICE\_1097 less  
0.258ns M\_SET requirement (totaling 2.700ns) by 5.373ns

Clock delay – Mini setup time =  $2.958 - 0.258 = 2.7\text{ns}$  (Be allowed mini data delay).

Data delay - Offset =  $2.327 - 5 = -2.673\text{ns}$  (Totaling data delay).

$2.7 - (-2.673) = 5.373\text{ns}$ .



# HOLD TIME REPORT

```
Preference: INPUT_SETUP PORT "test_in_pin[7]" 5.000000 ns HOLD 5.000000 ns CLKPORT "rclk_in" ;  
1 item scored, 0 timing errors detected.
```

---

Passed: The following path meets requirements by 4.436ns

```
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)  
  
Source: Port Pad test_in_pin[7]  
Destination: FF Data in test_in_reg_0io[7] (to rclk_in_c +)  
  
Min Data Path Delay: 0.816ns (58.6% logic, 41.4% route), 1 logic levels.  
Max Clock Path Delay: 1.399ns (38.1% logic, 61.9% route), 1 logic levels.
```

## Constraint Details:

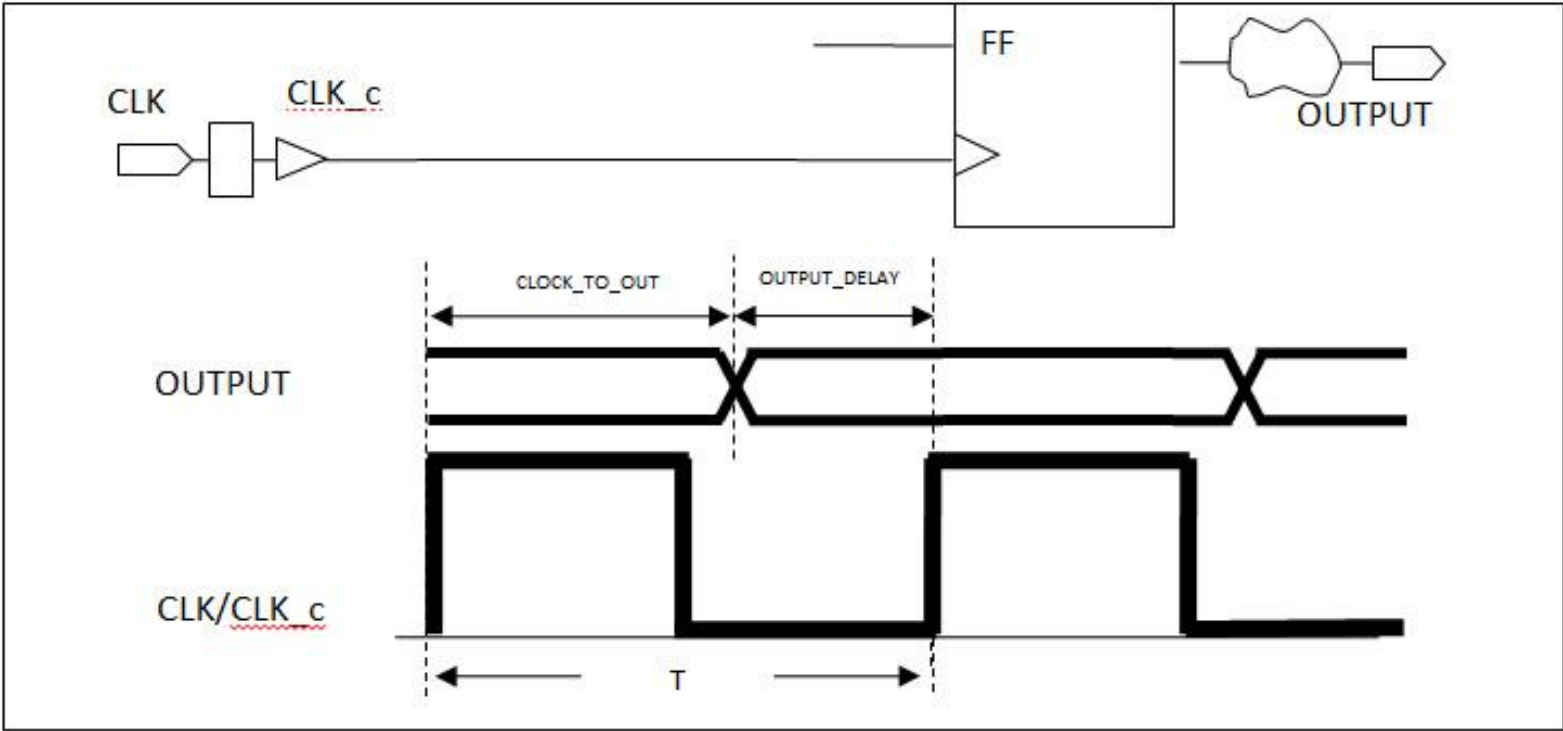
```
0.816ns delay test_in_pin[7] to SLICE_1097 plus  
5.000ns hold offset test_in_pin[7] to rclk_in (totaling 5.816ns) meets  
1.399ns delay rclk_in to SLICE_1097 plus  
-0.019ns M_HLD requirement (totaling 1.380ns) by 4.436ns
```

Clock delay + Mini hold time =  $1.399 + (-0.019) = 1.38\text{ns}$  ( Be allowed mini data delay).

Data delay + Hold offset =  $0.816 + 5 = 5.816\text{ns}$ .

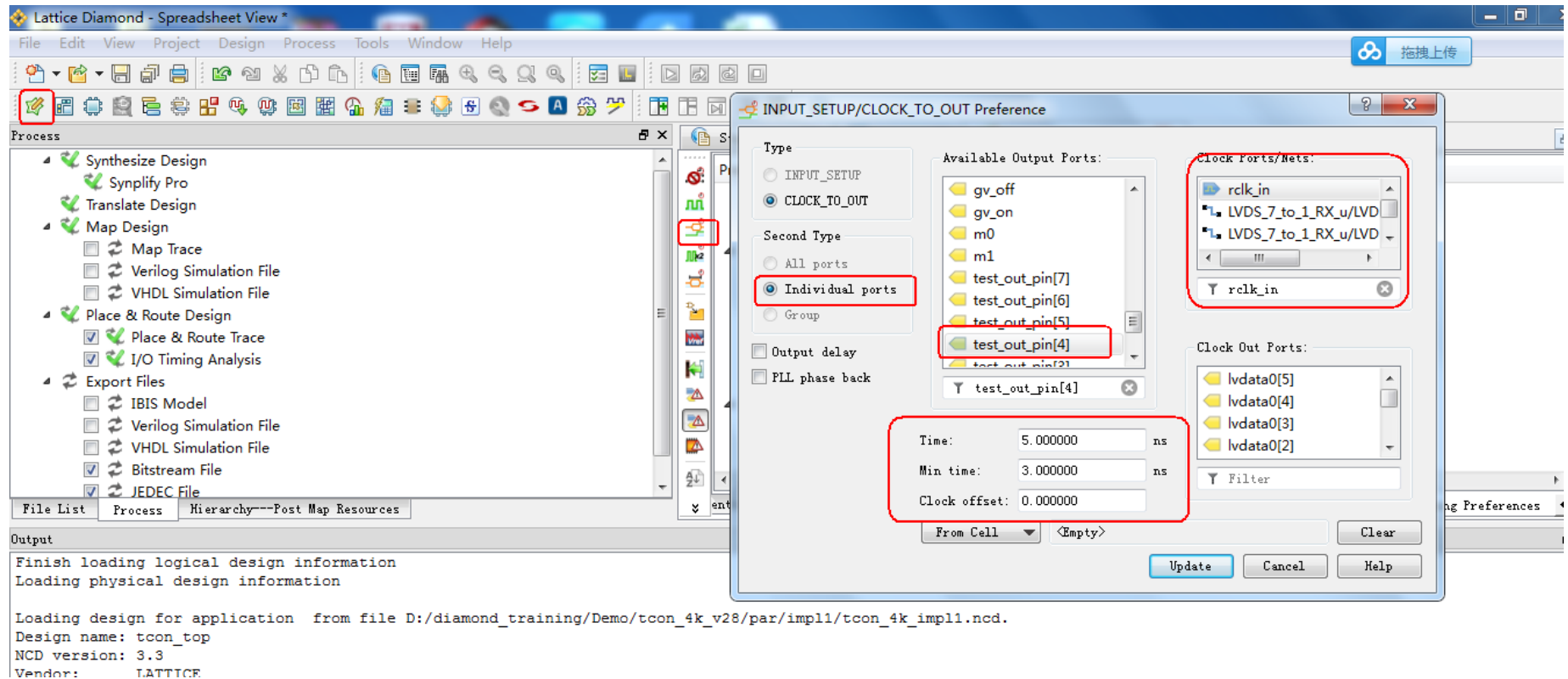
$5.816 - 1.38 = 4.436\text{ns}$ .

# CLOCK TO OUT



Clock to out + Output delay = T

# ADD CLOCK TO OUT CONSTRAINT



File Edit View Project Design Process Tools Window Help

Process

- Synthesize Design
  - Synplify Pro
- Translate Design
- Map Design
  - Map Trace
  - Verilog Simulation File
  - VHDL Simulation File
- Place & Route Design
  - Place & Route Trace
  - I/O Timing Analysis
- Export Files
  - IBIS Model
  - Verilog Simulation File
  - VHDL Simulation File
  - Bitstream File
  - JEDEC File

File List Process Hierarchy---Post Map Resources

Output

Finish loading logical design information  
Loading physical design information

Loading design for application from file D:/diamond\_training/Demo/tcon\_4k\_v28/par/impl1/tcon\_4k\_impl1.ncd.  
Design name: tcon\_top  
NCD version: 3.3  
Vendor: LATTICE

INPUT\_SETUP/CLOCK\_TO\_OUT Preference

Type

- INPUT\_SETUP
- CLOCK\_TO\_OUT

Second Type

- All ports
- Individual ports
- Group

Output delay

PLL phase back

Available Output Ports:

- gv\_off
- gv\_on
- m0
- m1
- test\_out\_pin[7]
- test\_out\_pin[6]
- test\_out\_pin[5]
- test\_out\_pin[4]
- test\_out\_pin[3]

Clock Ports/Nets:

- rclk\_in
- LVDS\_7\_to\_1\_RX\_u/LVD
- LVDS\_7\_to\_1\_RX\_u/LVD

Clock Out Ports:

- lvdata0[5]
- lvdata0[4]
- lvdata0[3]
- lvdata0[2]

Filter

Time: 5.000000 ns

Min time: 3.000000 ns

Clock offset: 0.000000

From Cell <Empty>

Update Cancel Help

Click Spreadsheet > Click Timing preferences > input setup/clock to out >

```
CLOCK_TO_OUT PORT "test_out_pin[4]" 5.000000 ns MIN 3.000000 ns CLKPORT "rclk_in";
```

# SETUP TIME REPORT

```
Preference: CLOCK_TO_OUT PORT "test_out_pin[4]" 5.000000 ns MIN 3.000000 ns CLKPORT "rclk_in" ; Setup Analysis.  
1 item scored, 1 timing error detected.
```

-----

Error: The following path exceeds requirements by 2.229ns

Logical Details:	Cell type	Pin type	Cell/ASIC name	(clock net +/-)
Source:	FF	Q	test_out_reg[4]&r3	(from rclk_in_c +)
Destination:	Port	Pad	test_out_pin[4]	

Data Path Delay: 3.984ns (98.9% logic, 1.1% route), 2 logic levels.

Clock Path Delay: 3.245ns (34.6% logic, 65.4% route), 1 logic levels.

Constraint Details:

3.245ns delay rclk\_in to test\_out\_pin[4]\_MGIOL and  
3.984ns delay test\_out\_pin[4]\_MGIOL to test\_out\_pin[4] (totaling 7.229ns) exceeds  
5.000ns offset rclk\_in to test\_out\_pin[4] by 2.229ns

Clock delay + Data delay = 3.245 + 3.984 = 7.229ns.

7.229 – 5 = 2.229ns.

# HOLD TIME REPORT

```
Preference: CLOCK_TO_OUT PORT "test_out_pin[4]" 5.000000 ns MIN 3.000000 ns CLKPORT "rclk_in" ;  
1 item scored, 1 timing error detected.
```

-----  
Error: The following path exceeds requirements by 0.443ns

```
Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)  
Source: FF Q test_out_reg[4]#r3 (from rclk_in_c +)  
Destination: Port Pad test_out_pin[4]
```

```
Data Path Delay: 1.278ns (99.1% logic, 0.9% route), 2 logic levels.
```

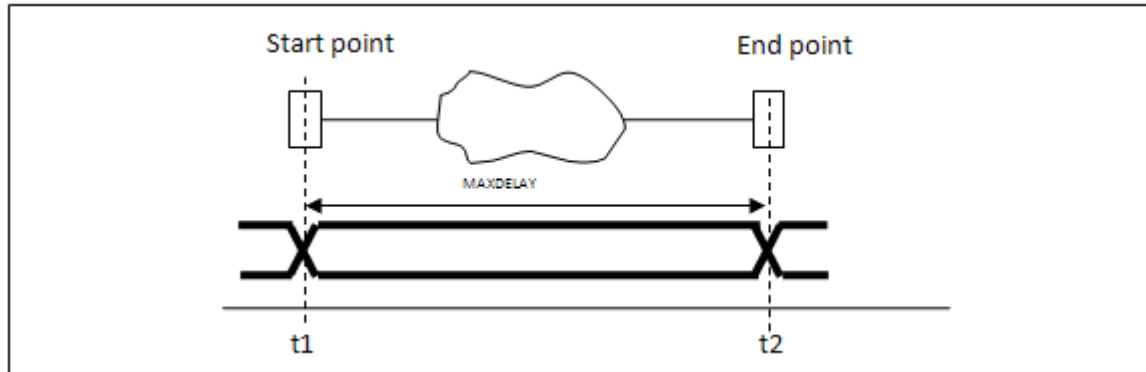
```
Clock Path Delay: 1.279ns (36.5% logic, 63.5% route), 1 logic levels.
```

Constraint Details:

```
1.279ns delay rclk_in to test_out_pin[4]_MGIOL and  
1.278ns delay test_out_pin[4]_MGIOL to test_out_pin[4] (totaling 2.557ns) exceeds  
3.000ns hold offset rclk_in to test_out_pin[4] by 0.443ns
```

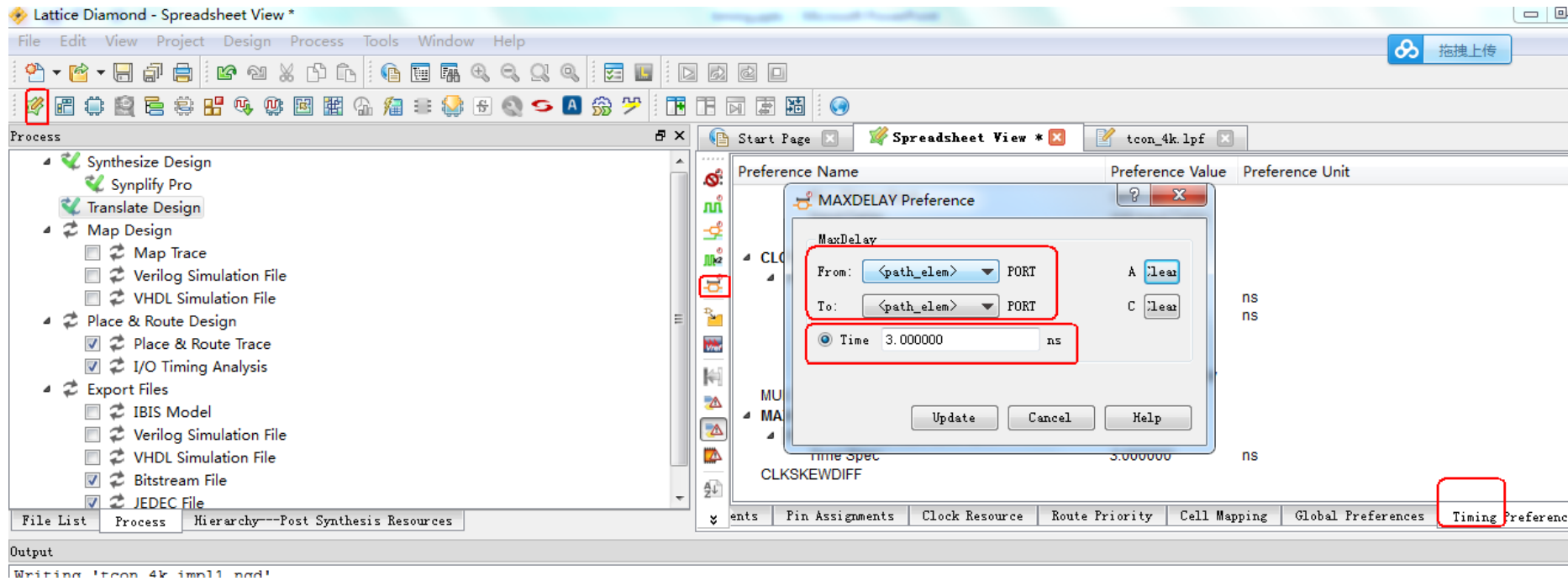
Clock delay + data delay = 1.279 + 1.278 = 2.557ns.

2.557 – 3 = -0.443ns.



- When a net is specified, the maximum delay constraint applies to all driver-to-load connections on the net.
- When a path is specified, the delay value is the constraint for the path including net and component delays as defined by the path spec rules.

# ADD MAXDELAY CONSTRAINT



Preference Name	Preference Value	Preference Unit
MAXDELAY Preference		
MaxDelay		
From: <path_elem> PORT	A	ns
To: <path_elem> PORT	C	ns
Time 3.000000		ns
Update	Cancel	Help
Time Spec	3.000000	ns
CLKSKEWDIFF		

Spreadsheet > Timing preferences > MAXDELAY >

MAXDELAY FROM PORT "A" TO PORT "C" 3.000000 ns ;

MAXDELAY NET "\*/dq\_read\_o\_p01\*" 0.550000 ns ;

# SETUP TIME REPORT

```
=====
Preference: MAXDELAY FROM PORT "A" TO PORT "C" 3.000000 ns ;
          1 item scored, 1 timing error detected.
-----
```

Error: The following path exceeds requirements by 4.991ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

```
Source:      Port      Pad      A
Destination: Port      Pad      C
```

Delay: 7.991ns (65.4% logic, 34.6% route), 3 logic levels.

Constraint Details:

```
7.991ns physical path delay A to C exceeds
3.000ns delay constraint by 4.991ns
```

Physical Path Details:

Data path A to C:

Name	Fanout	Delay (ns)	Site	Resource
PADI_DEL	---	1.372	N8.PAD to	N8.PADDI A
ROUTE	1	1.490	N8.PADDI to	R21C12C.C1 A_c
CTOF_DEL	---	0.408	R21C12C.C1 to	R21C12C.F1 SLICE_769
ROUTE	1	1.273	R21C12C.F1 to	U5.PADDO C_c
DOPAD_DEL	---	3.448	U5.PADDO to	U5.PAD C

```
-----
7.991 (65.4% logic, 34.6% route), 3 logic levels.
```

Warning: 7.991ns is the maximum delay for this preference.



# HOLD TIME REPORT

Preference: CLOCK\_TO\_OUT PORT "test\_out\_pin[4]" 5.000000 ns MIN 3.000000 ns CLKPORT "rclk\_in" ;  
1 item scored, 1 timing error detected.

-----

Error: The following path exceeds requirements by 0.386ns

Logical Details: Cell type Pin type Cell/ASIC name (clock net +/-)

Source: FF Q test\_out\_reg[4] (from rclk\_in\_c +)  
Destination: Port Pad test\_out\_pin[4]

Data Path Delay: 1.399ns (87.0% logic, 13.0% route), 2 logic levels.  
Clock Path Delay: 1.215ns (38.4% logic, 61.6% route), 1 logic levels.

Constraint Details:

1.215ns delay rclk\_in to SLICE\_123 and  
1.399ns delay SLICE\_123 to test\_out\_pin[4] (totaling 2.614ns) exceeds  
3.000ns hold offset rclk\_in to test\_out\_pin[4] by 0.386ns

Physical Path Details:

Clock path rclk\_in to SLICE\_123:

Name	Fanout	Delay (ns)	Site	Resource
PADI_DEL	---	0.467	V10.PAD to	V10.PADDI rclk_in
ROUTE	38	0.748	V10.PADDI to	R25C28C.CLK rclk_in_c

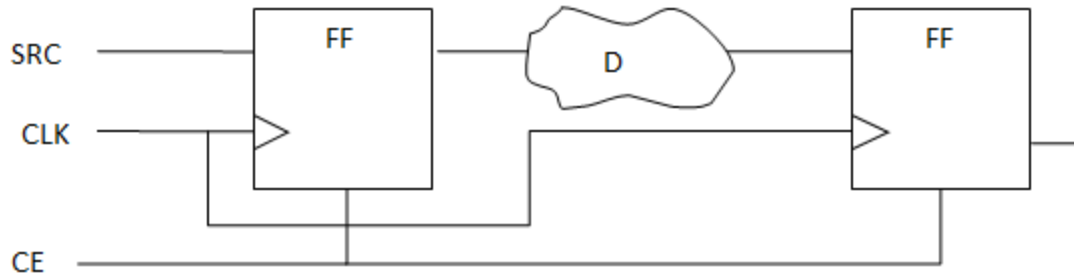
-----  
1.215 (38.4% logic, 61.6% route), 1 logic levels.

Data path SLICE\_123 to test\_out\_pin[4]:

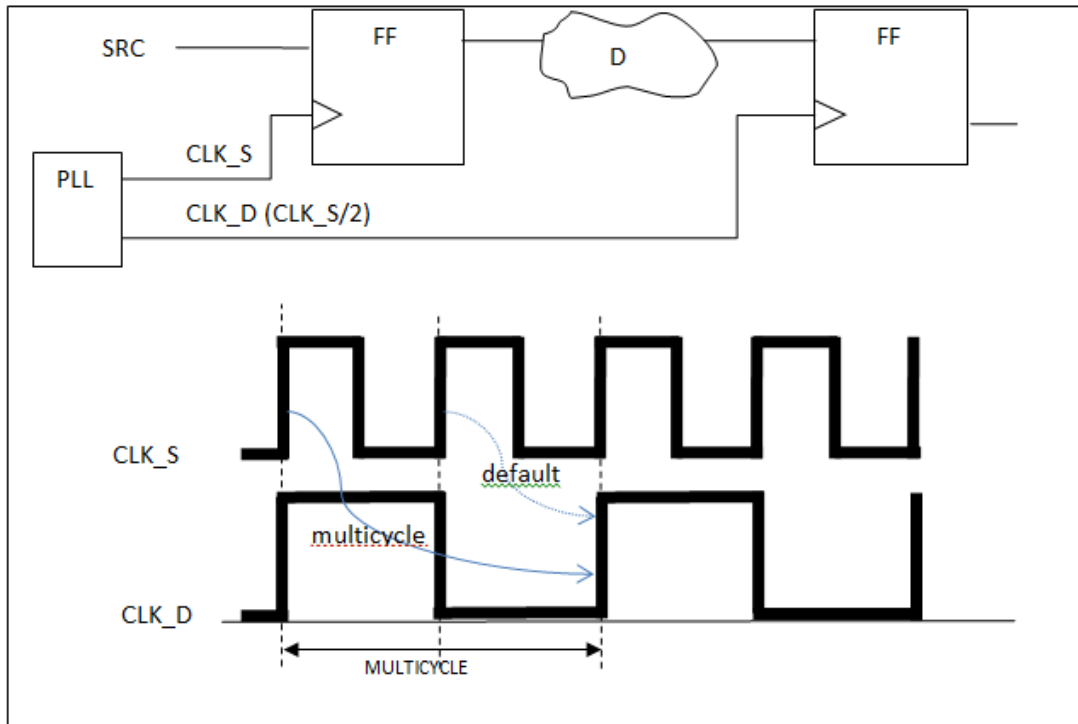
Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.133	R25C28C.CLK to	R25C28C.Q1 SLICE_123 (from rclk_in_c)
ROUTE	2	0.182	R25C28C.Q1 to	P11.PADD0 test_cntf[12]
DOPAD_DEL	---	1.084	P11.PADD0 to	P11.PAD test_out_pin[4]

-----  
1.399 (87.0% logic, 13.0% route), 2 logic levels.

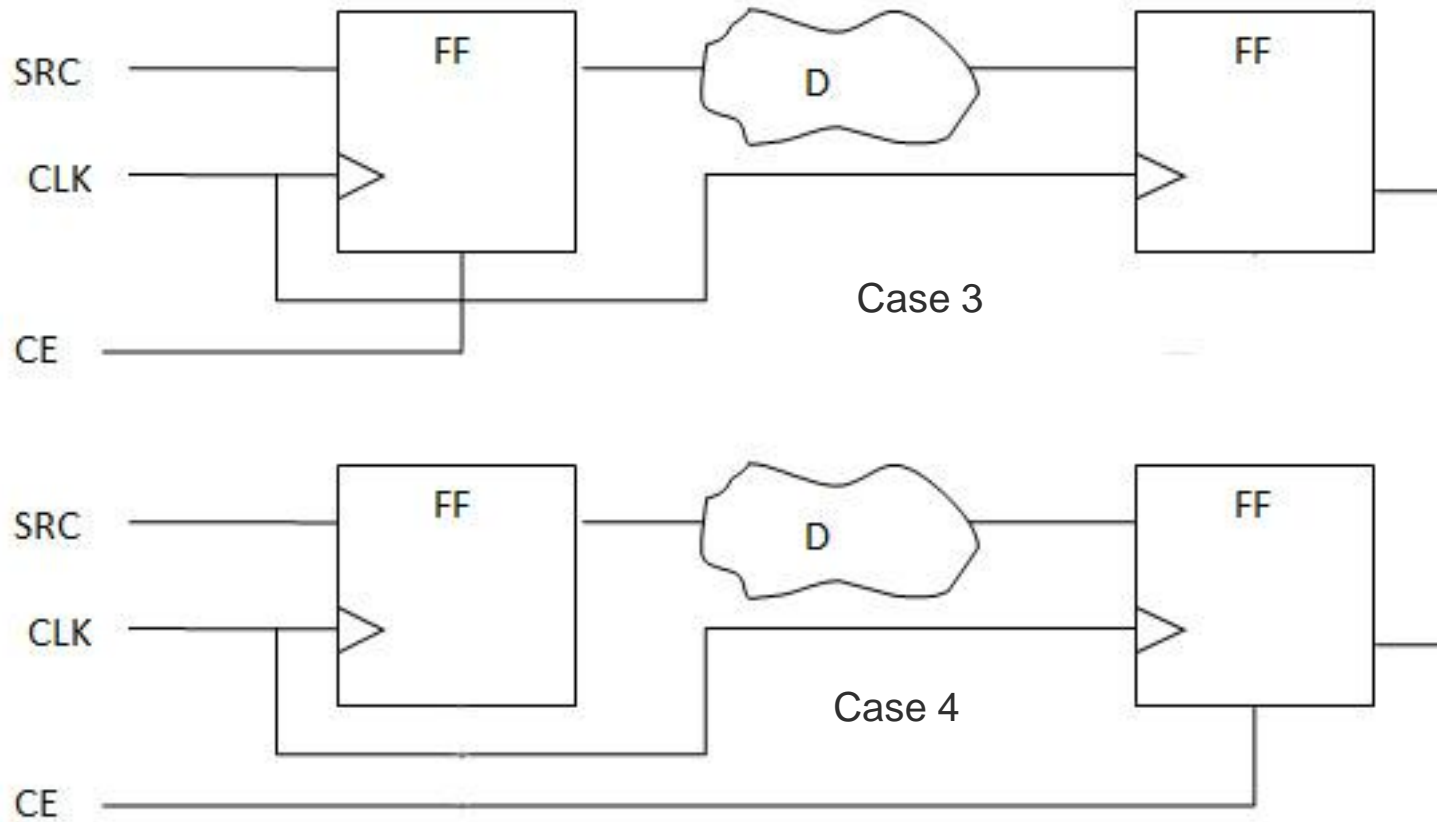
Warning: 2.614ns is the maximum offset for this preference.



Case 1:  
 CE is multi cycle signal.  
 Can use multicycle between source FF and destination FF.

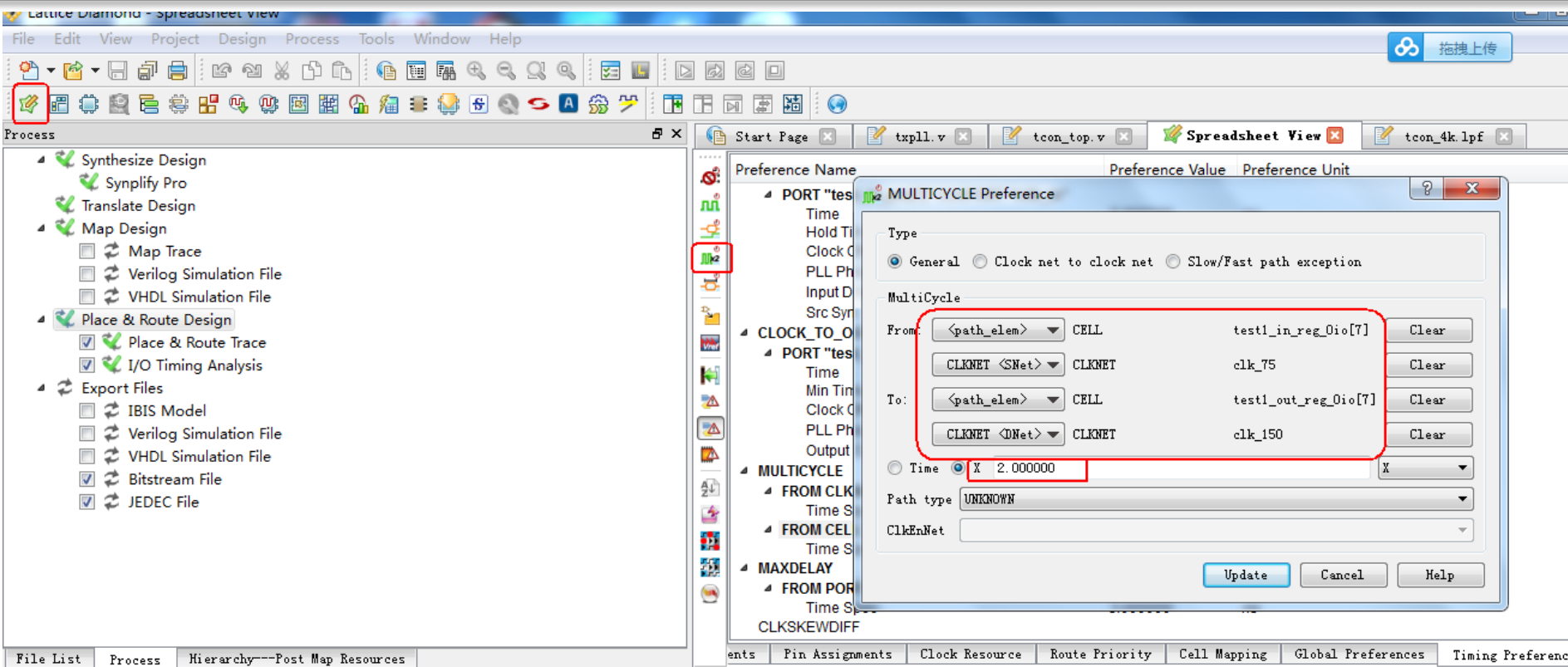


Case 2:  
 Data will be changed every CLK\_S, and data will be changed every odd CLK\_S.  
 can't use multicycle.  
 Data will be changed every even CLK\_S  
 Can use multicycle.



Even CE is multi cycle, can't use multicycle constraint for case 3 and case 4.

# ADD MULTICYCLE CONSTRAINT



The screenshot shows the Lattice Diamond software interface in Spreadsheet View. The 'MULTICYCLE Preference' dialog box is open, showing the following configuration:

- Type:  General
- MultiCycle:
  - From:  CELL test1\_in\_reg\_0io[7] Clear
  - CLKNET <SNet> CLKNET clk\_75 Clear
  - To:  CELL test1\_out\_reg\_0io[7] Clear
  - CLKNET <DNet> CLKNET clk\_150 Clear
- Time:  X 2.000000 X
- Path type: UNKNOWN
- ClkEnNet: [Empty]

Buttons: Update, Cancel, Help

Spreadsheet > Timing preferences > MULTICYCLE >

MULTICYCLE FROM CLKNET "clk\_75" TO CLKNET "clk\_150" 2.000000 X ;

MULTICYCLE FROM CELL "test1\_in\_reg\_0io[7]" CLKNET "clk\_75" TO CELL "test1\_out\_reg\_0io[7]" CLKNET "clk\_150" 2.000000 X ;

# SETUP TIME REPORT

```
=====
Preference: MULTICYCLE FROM CLKNET "clk_75" TO CLKNET "clk_150" 2.000000 X ;
          7 items scored, 0 timing errors detected.
-----
```

Passed: The following path meets requirements by 11.161ns

```
Logical Details:  Cell type  Pin type      Cell/ASIC name  (clock net +/-)
Source:          FF          Q          test1_in_reg_0io[1]  (from clk_75 +)
Destination:    FF          Data in    test1_out_reg_0io[1] (to clk_150 +)

Delay:           2.151ns  (17.1% logic, 82.9% route), 1 logic levels.
```

#### Constraint Details:

```
2.151ns physical path delay SLICE_59 to test1_out_pin[1]_MGIOL meets
13.334ns delay constraint less
-0.099ns skew and
0.000ns feedback compensation and
0.121ns DO_SET requirement (totaling 13.312ns) by 11.161ns
```

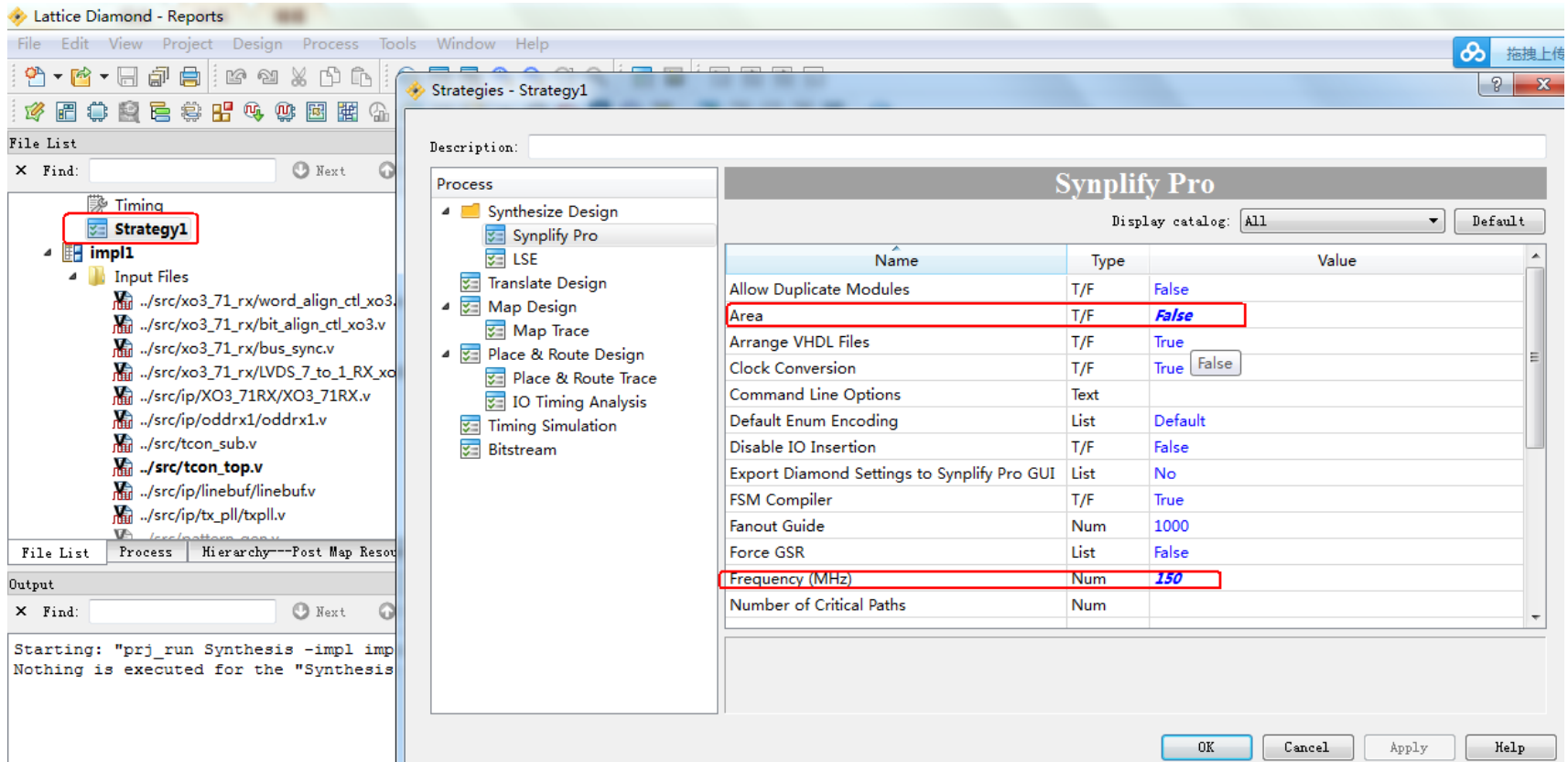
$2T - \text{Skew} - \text{Mini setup time} = 13.334 - (-0.099) + 0.121 = 13.312\text{ns}$  (Be allowed max data delay).

$13.312 - 2.151 = 11.161\text{ns}$ .

- The following preference command blocks timing analysis on a net named n1:
  - BLOCK NET n1;
- The following preference command blocks timing analysis on all asynchronous set/reset paths, through an asynchronous set/reset pin on a design component.
  - BLOCK RESETPATHS;
- The following preference command blocks the path between two ports:
  - BLOCK PATH FROM PORT "LOCAL\_CMD0" TO PORT "RAM\_RD";
- The following preference blocks specific inter clock domains between clock nets. All maximum frequency (fMAX) paths from clknet\_1 to clknet\_2 will be blocked from timing analysis.
  - BLOCK PATH FROM CLKNET "clknet\_1 " TO CLKNET "clknet\_2 ";
- The following preference blocks all paths involving data transfer between registers that are clocked by different clock nets—even when those clock nets are related.
  - BLOCK INTERCLOCKDOMAIN PATHS ;

1. The top level should only contain instantiation statements to call all major blocks.
2. Keep related logic together in the same block.
3. Separate Logic with Different Optimization Goals.
4. The tri-state statement for all bidirectional ports should be written at the top-level module.
5. Maintain sub-blocks by registering all outputs.
6. Use case statement instead of If Else statement if it's possible.
7. Avoiding use Latches.
8. *Memory* and DSP with output register.
9. Pipelining long combination logic.
10. For cross clock Domain signal, double register or use FIFO.

# METHOD 1 OF TIMING CLOSURE



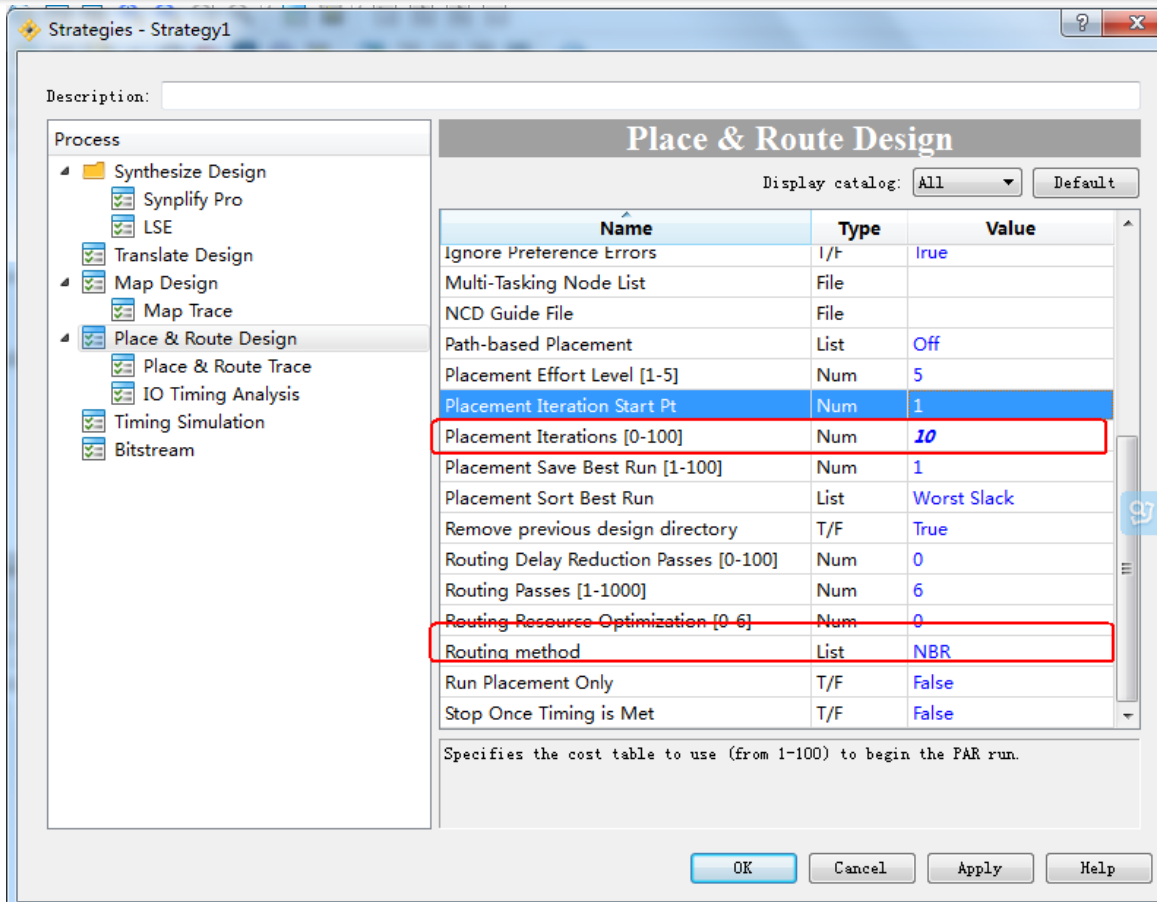
The screenshot shows the Lattice Diamond Reports window with the Synplify Pro settings dialog open. The 'Area' setting is set to False, and the 'Frequency (MHz)' setting is set to 150. The 'Process' tree on the left shows the Synplify Pro process selected.

Name	Type	Value
Allow Duplicate Modules	T/F	False
Area	T/F	False
Arrange VHDL Files	T/F	True
Clock Conversion	T/F	True <input type="checkbox"/>
Command Line Options	Text	
Default Enum Encoding	List	Default
Disable IO Insertion	T/F	False
Export Diamond Settings to Synplify Pro GUI	List	No
FSM Compiler	T/F	True
Fanout Guide	Num	1000
Force GSR	List	False
Frequency (MHz)	Num	150
Number of Critical Paths	Num	

Close area priority and set suitable frequency.

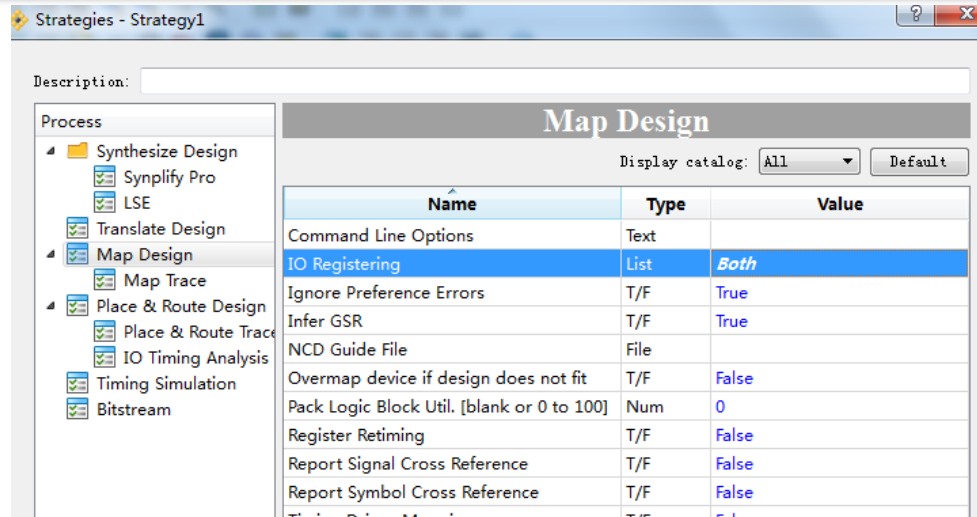


# METHOD 2 OF TIMING CLOSURE



- Using Multiple Placement Iterations.
- Try to use Routing method: NBR or CDR.

# METHOD 3 OF TIMING CLOSURE

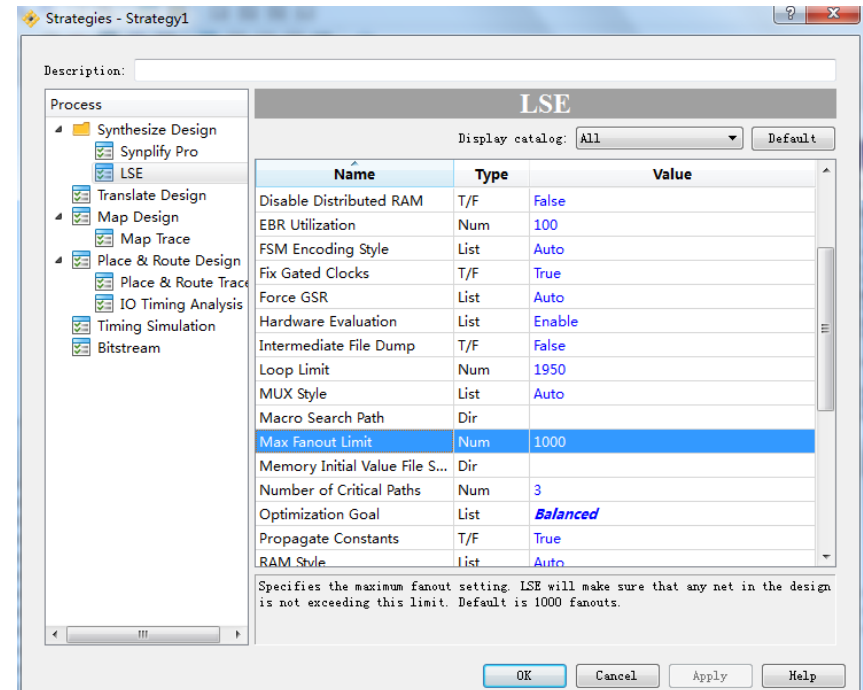
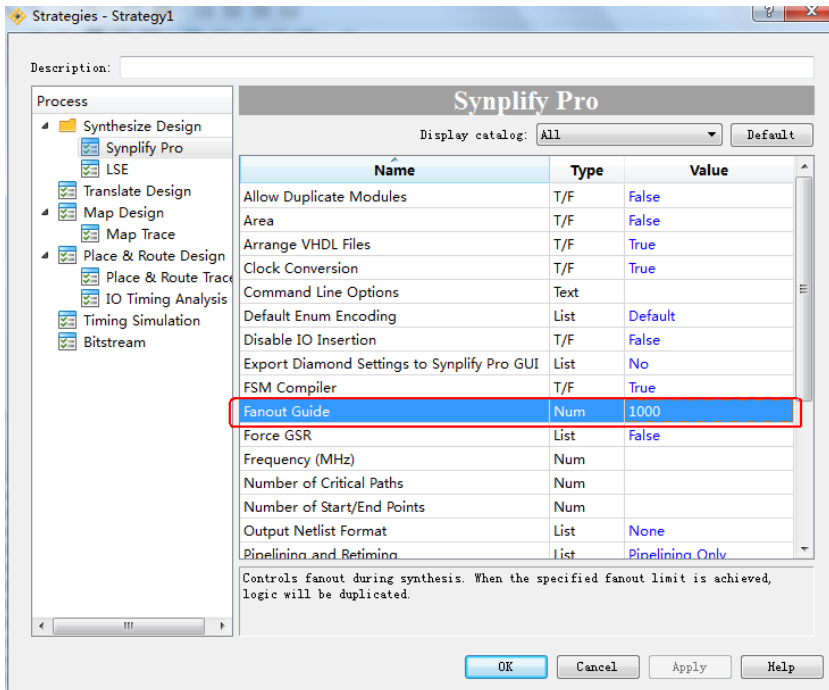


Data path tcon\_sub\_u/SLICE\_80 to tp\_MGIOL:

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.367	R15C18D.CLK to	R15C18D.Q1 tcon_sub_u/SLICE_80 (from clk_150)
ROUTE	9	2.182	R15C18D.Q1 to	R18C17C.B1 tcon_sub_u/hs_cnt[6]
CTOF_DEL	---	0.408	R18C17C.B1 to	R18C17C.F1 SLICE_797
ROUTE	3	1.163	R18C17C.F1 to	R17C18B.D0 tcon_sub_u/N_23
CTOF_DEL	---	0.408	R17C18B.D0 to	R17C18B.F0 SLICE_831
ROUTE	1	0.588	R17C18B.F0 to	R17C17A.C0 tcon_sub_u/N_47
CTOF_DEL	---	0.408	R17C17A.C0 to	R17C17A.F0 SLICE_791
ROUTE	1	2.468	R17C17A.F0 to	IOL_L23A.OPOS tcon_sub_u.N_9_i (to clk_150)
		7.992	(19.9% logic, 80.1% route), 4 logic levels.	

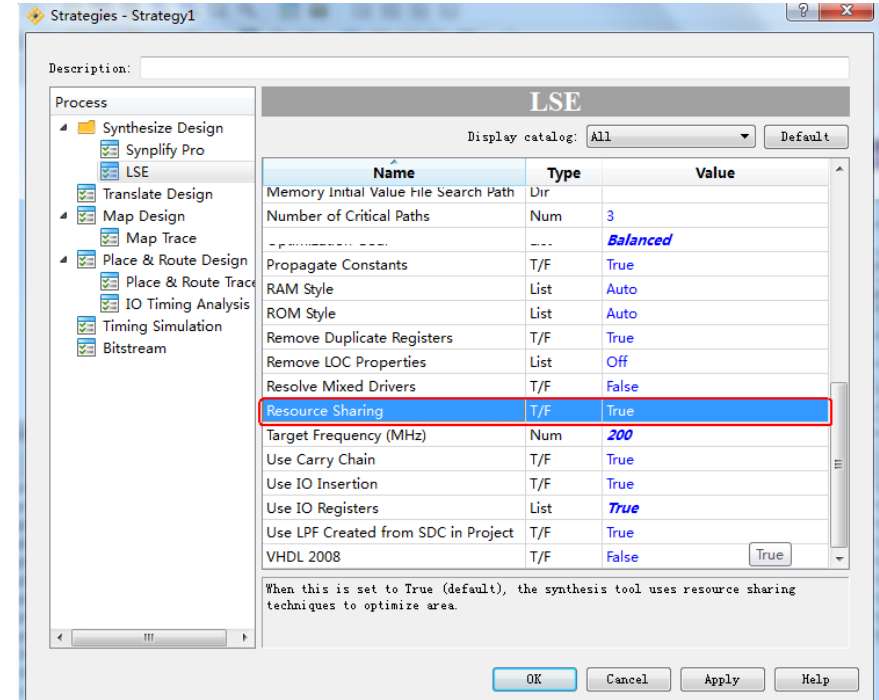
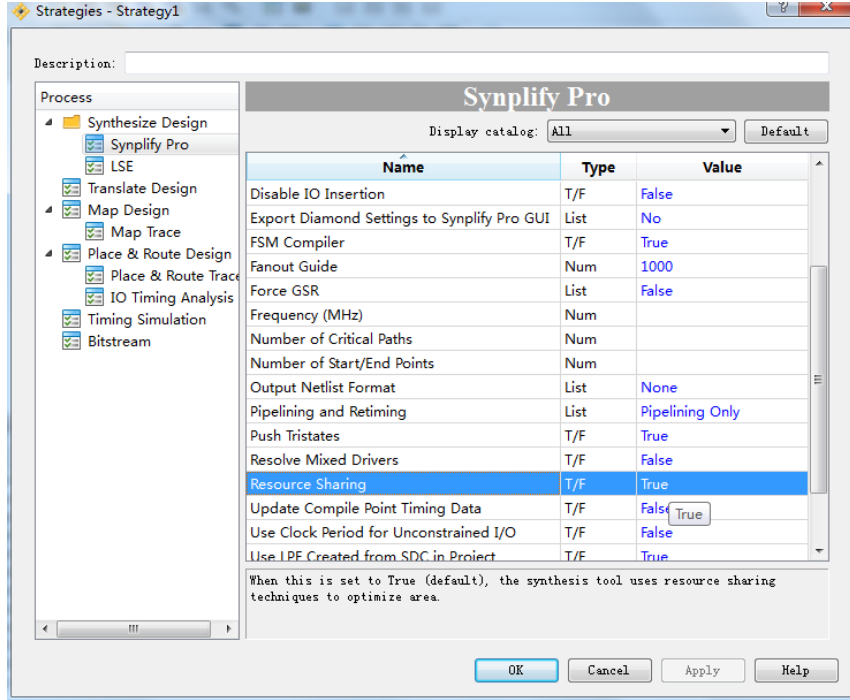
Using or not I/O register to improve I/O timing.  
 output [15:0] q /\* synthesis syn\_useioff = 1\*/;

# METHOD 4 OF TIMING CLOSURE



```
input [31: 0] data_in /* synthesis syn_maxfan= 100 */;  
reg [31:0] data_out /* synthesis syn_maxfan=10 */;
```

# METHOD 5 OF TIMING CLOSURE



```
module sub_module
(
  input [7:0] inA, input [7:0] inB,
  input clk, input sel1, input sel2,
  input rst, output [15:0] outB
)/*synthesis syn_sharing = 0*/;
```

# METHOD 6 OF TIMING CLOSURE

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.367	R11C13A.CLK to	R11C13A.Q1 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/SLICE_808 (from rx_sclk)
ROUTE	4	1.307	R11C13A.Q1 to	R11C13D.D0 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/cur_stable_rxclk_word[1]
CTOF_DEL	---	0.408	R11C13D.D0 to	R11C13D.F0 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/SLICE_786
ROUTE	1	1.840	R11C13D.F0 to	R11C13D.B1 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/r_ml_e_1_1
CTOF_DEL	---	0.408	R11C13D.B1 to	R11C13D.F1 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/SLICE_786
ROUTE	1	0.501	R11C13D.F1 to	R11C12B.D0 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/r_ml_e_1
CTOF_DEL	---	0.408	R11C12B.D0 to	R11C12B.F0 SLICE_806
ROUTE	1	1.550	R11C12B.F0 to	R14C12A.C1 LVDS_7_to_1_RX_u/bit_aln_ctl_inst/r_N_3_mux
CTOF_DEL	---	0.408	R14C12A.C1 to	R14C12A.F1 SLICE_787
ROUTE	4	1.220	R14C12A.F1 to	R17C13D.CE LVDS_7_to_1_RX_u/bit_aln_ctl_inst/un1_dphase_cnt19_10_i (to rx_sclk)

-----  
8.417 (23.7% logic, 76.3% route), 5 logic levels.

```
reg [7:0] Dout /* synthesis syn_useenables = 0*/;
```

# METHOD 7 OF TIMING CLOSURE

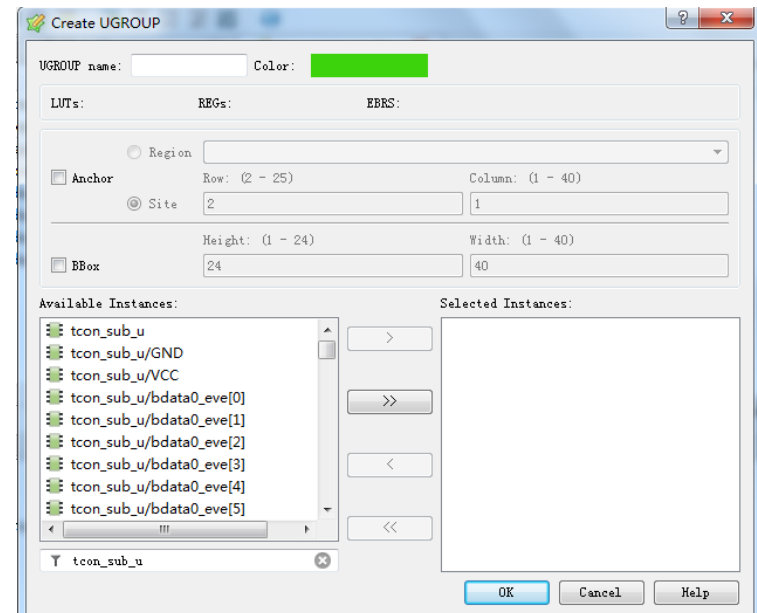
```
Name Fanout Delay (ns) Site Resource
REG_DEL --- 0.243 R81C10C.CLK to R81C10C.Q1 U_top/module_A/submodule_B/SLICE_2
(from sys_clk)
ROUTE 3 0.516 R81C10C.Q1 to R81C12D.D0 U_top/module_A/submodule_B/
col_count_4
CTOF_DEL --- 0.147 R81C12D.D0 to R81C12D.F0 U_top/module_A/submodule_B/
SLICE_25670
ROUTE 1 0.255 R81C12D.F0 to R81C12D.C1 U_top/module_A/submodule_B/
m27_e_s_10_1
CTOF_DEL --- 0.147 R81C12D.C1 to R81C12D.F1 U_top/module_A/SLICE_25670
ROUTE 1 0.562 R81C12D.F1 to R81C14A.A1 U_top/module_A/m27_s_10_1
CTOF_DEL --- 0.147 R81C14A.A1 to R81C14A.F1 U_top/module_A/SLICE_9269
ROUTE 9 2.602 R81C14A.F1 to R57C49C.D1 N_150822
CTOF_DEL --- 0.147 R57C49C.D1 to R57C49C.F1 SLICE_23827
ROUTE 1 1.949 R57C49C.F1 to R75C25C.M1 U_top/module_A/dout_9_0_i_4
(to sys_clk)

-----
6.715 (12.4% logic, 87.6% route), 5 logic levels.
```

ROUTE 9 2.602 R81C14A.F1 to R57C49C.D1 N\_150822  
CTOF\_DEL --- 0.147 R57C49C.D1 to R57C49C.F1 SLICE\_23827  
ROUTE 1 1.949 R57C49C.F1 to R75C25C.M1 U\_top/module\_A/dout\_9\_0\_i\_4  
(to sys\_clk)

```
module moduleA(CLK, A, B, Y)
/* synthesis UGROUP="MODULE_A" */;

Maybe you need move the PGROUP from *.prffile.
```



# METHOD 8 OF TIMING CLOSURE

Name	Fanout	Delay (ns)	Site	Resource
REG_DEL	---	0.243	R51C141C.CLK to	R51C141C.Q0 SLICE_15 (from CLK_c)
ROUTE	12	0.760	R51C141C.Q0 to	R51C143A.A0 tmp1_0
CTOF_DEL	---	0.147	R51C143A.A0 to	R51C143A.F0 B_1_CR7_ram_0/SLICE_9
ROUTE	1	2.725	R75C143A.F0 to	R75C142C.B1 B_1_4
ClTOFCO_DE	---	0.277	R75C142C.B1 to	R75C142C.FCO SLICE_3
ROUTE	1	0.000	R75C142C.FCO to	R75C143A.FCI Y_1_cry_4
FCITOF1_DE	---	0.177	R75C143A.FCI to	R75C143A.F1 SLICE_4
ROUTE	1	0.811	R75C143A.F1 to	IOL_R52A.OPOSA Y_1_6 (to CLK_c)

-----  
 5.140(17.9% logic, 83.1% route), 4 logic levels.

```

reg [7:0] A_d1, A_d2, A_d3, A_d4 /* synthesis syn_srlstyle = "registers" */;
reg [7:0] B_d1, B_d2, B_d3, B_d4 /* synthesis syn_srlstyle = "registers" */;
always @(posedge CLK)
begin
  A_d1 <= A;
  B_d1 <= B;
  A_d2 <= A_d1;
  B_d2 <= B_d1;
  A_d3 <= A_d2;
  B_d3 <= B_d2;
  A_d4 <= A_d3;
  B_d4 <= B_d3;
end
  
```

Using Register instead of memory shift

# METHOD 9 OF TIMING CLOSURE

You can also LOCATE a given UGROUP at a particular site. The specified site can be a slice site or an EBR site. If you use a slice site, the slice name must end with the letter D.

Example, LOCATE register “de\_pre2” to R10C8D:

```
UGROUP "de_pre2" BLKNAME tcon_sub_u/de_pre2_389;
```

```
LOCATE UGROUP "de_pre2" SITE "R10C8D" ;
```

```
Netlist View | NCD View | tcon_sub.v
```

```
parameter GOE_END = 12'd1600;
```

```
reg vs_pre1;
```

```
reg vs_pre2;
```

```
reg hs_pre1;
```

```
reg hs_pre2;
```

```
reg de_pre1;
```

```
reg de_pre2;
```

```
wire vs_pos;
```

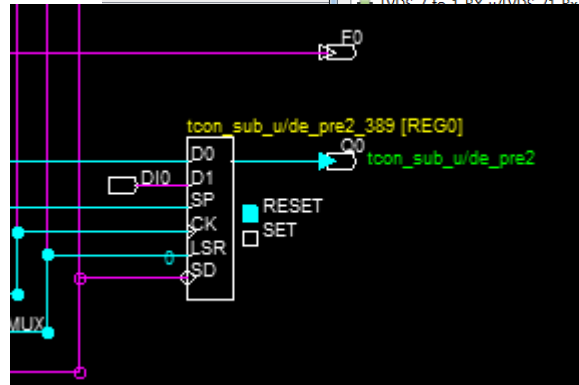
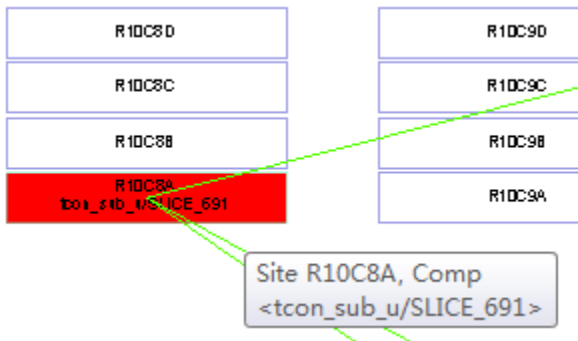
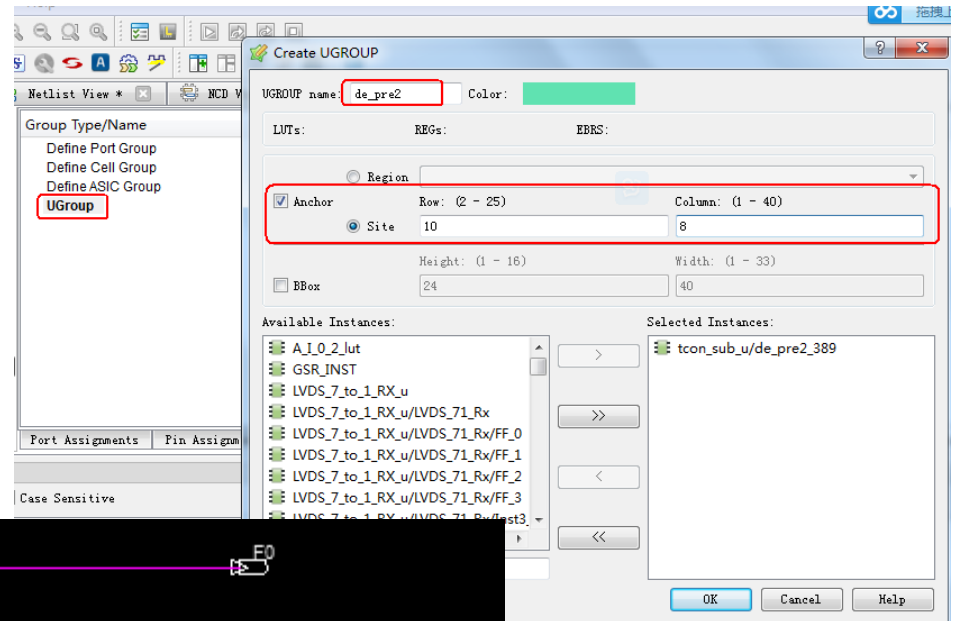
```
wire vs_neg;
```

```
wire hs_pos;
```

```
wire hs_neg;
```

```
wire de_pos;
```

```
wire de_neg;
```





**Modify source code!**